Circuit Architecture for VTL with MLC Flash Transistor

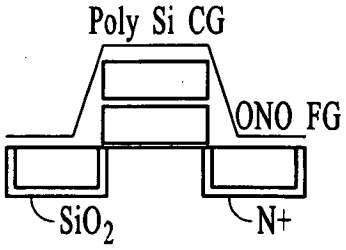


FIG.1A

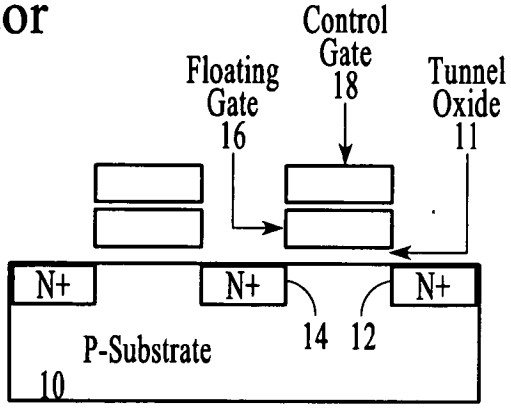


FIG.1A'

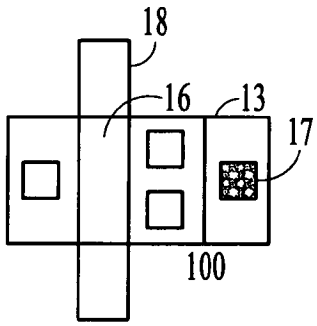


FIG.1B

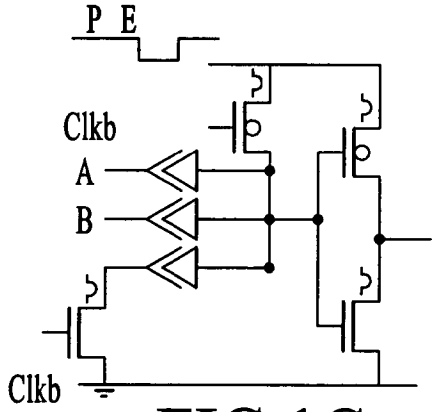


FIG.1C

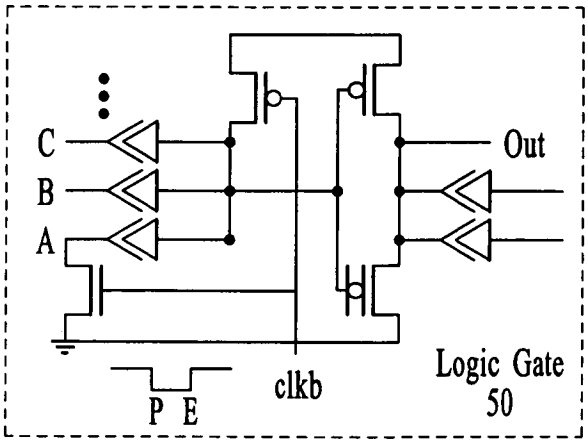


FIG.1D

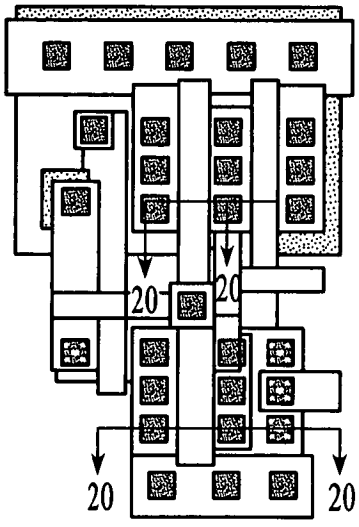
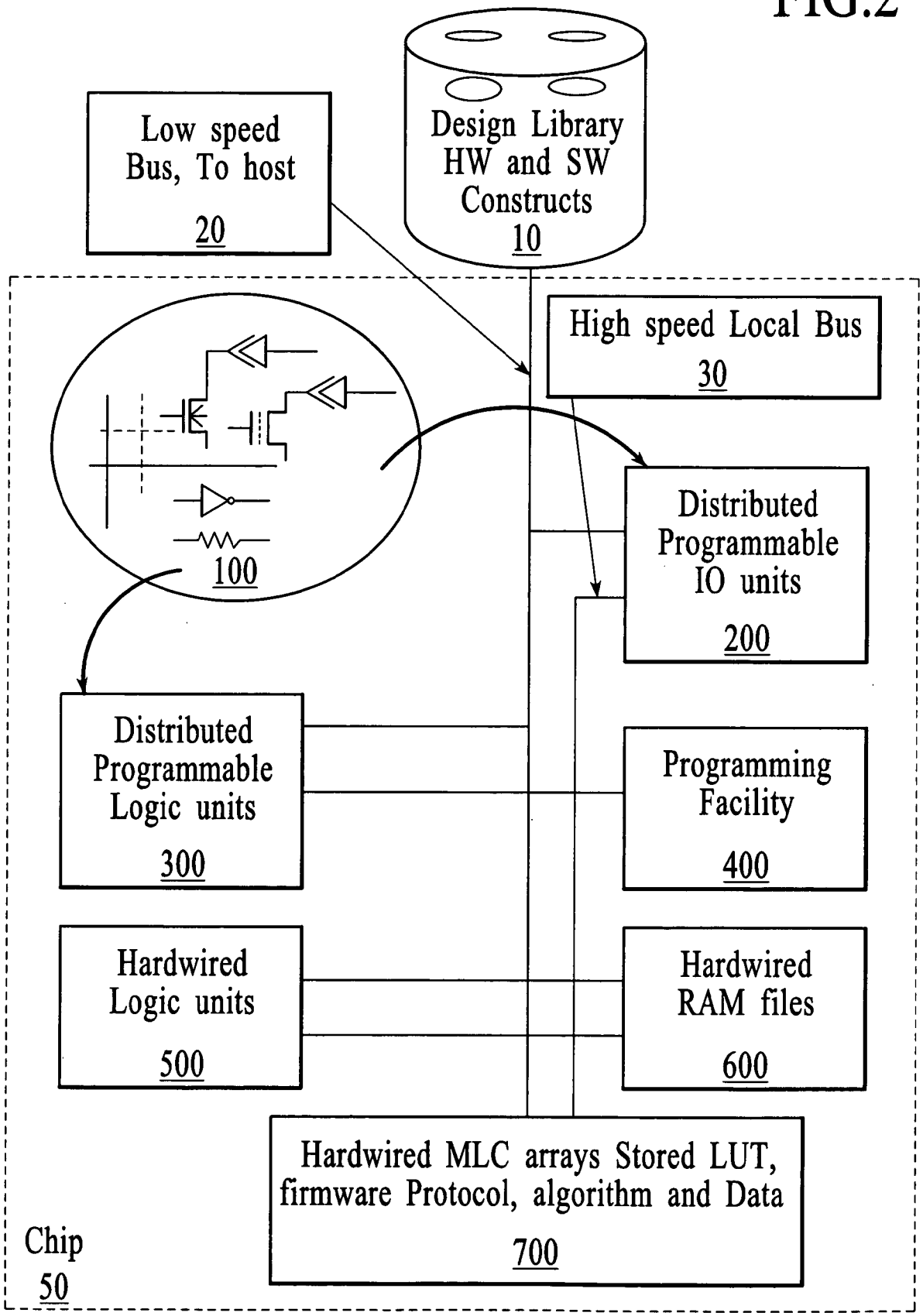


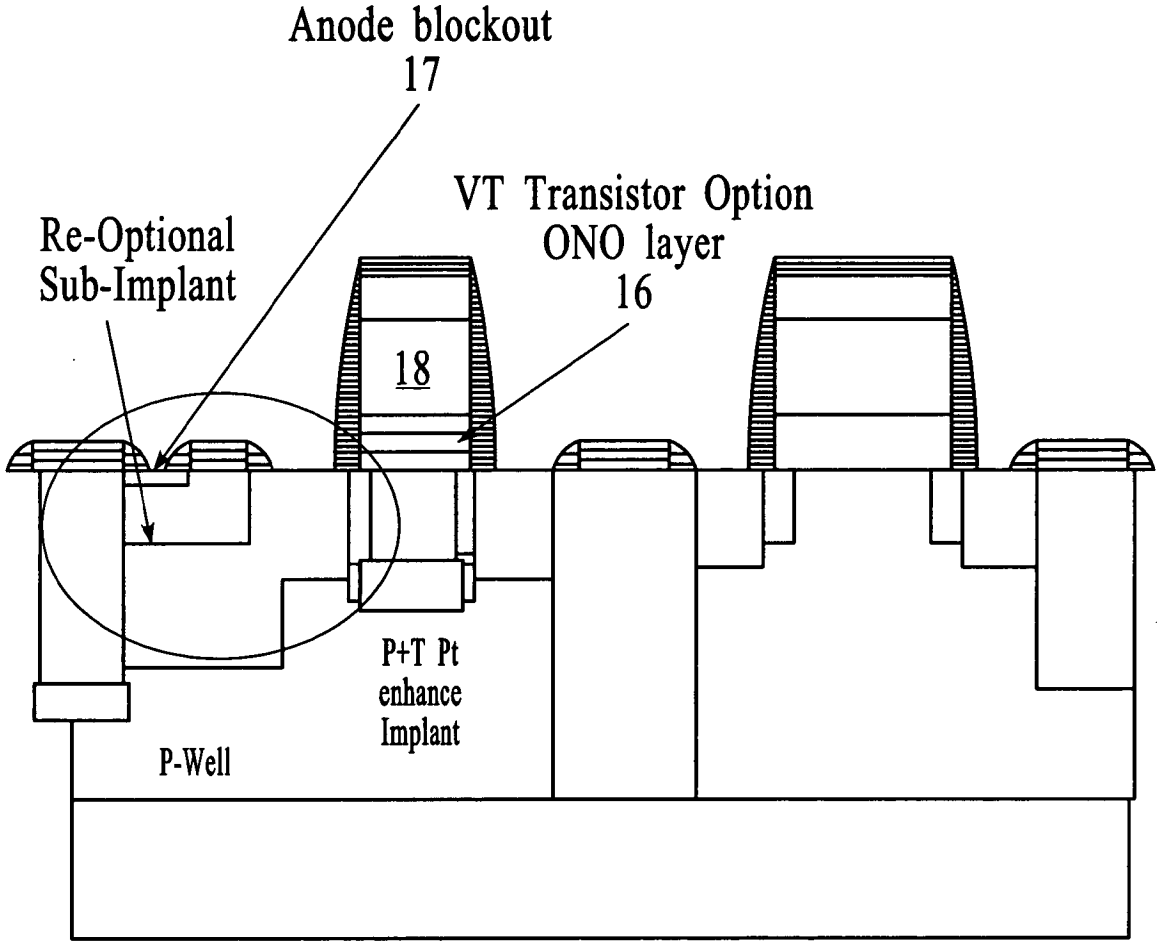
FIG.1E

System Architecture of VTL and MLC arrays

FIG.2



- Integrated Schottky-CFET cross section view
- *SBD special:* Anode implant block out, barrier metal, and Cathode bulk resistance implant



Standard processes: Conventional Trench/ROX Isolation, CMOS transistors, and post contact metal processes

FIG.3

SBD IF vs VF

- Diode curves at -0, 25, 85 aC junction
- R ~ 1.5KΩ for I<100 uA, R ~ 150Ω for I<1 mA

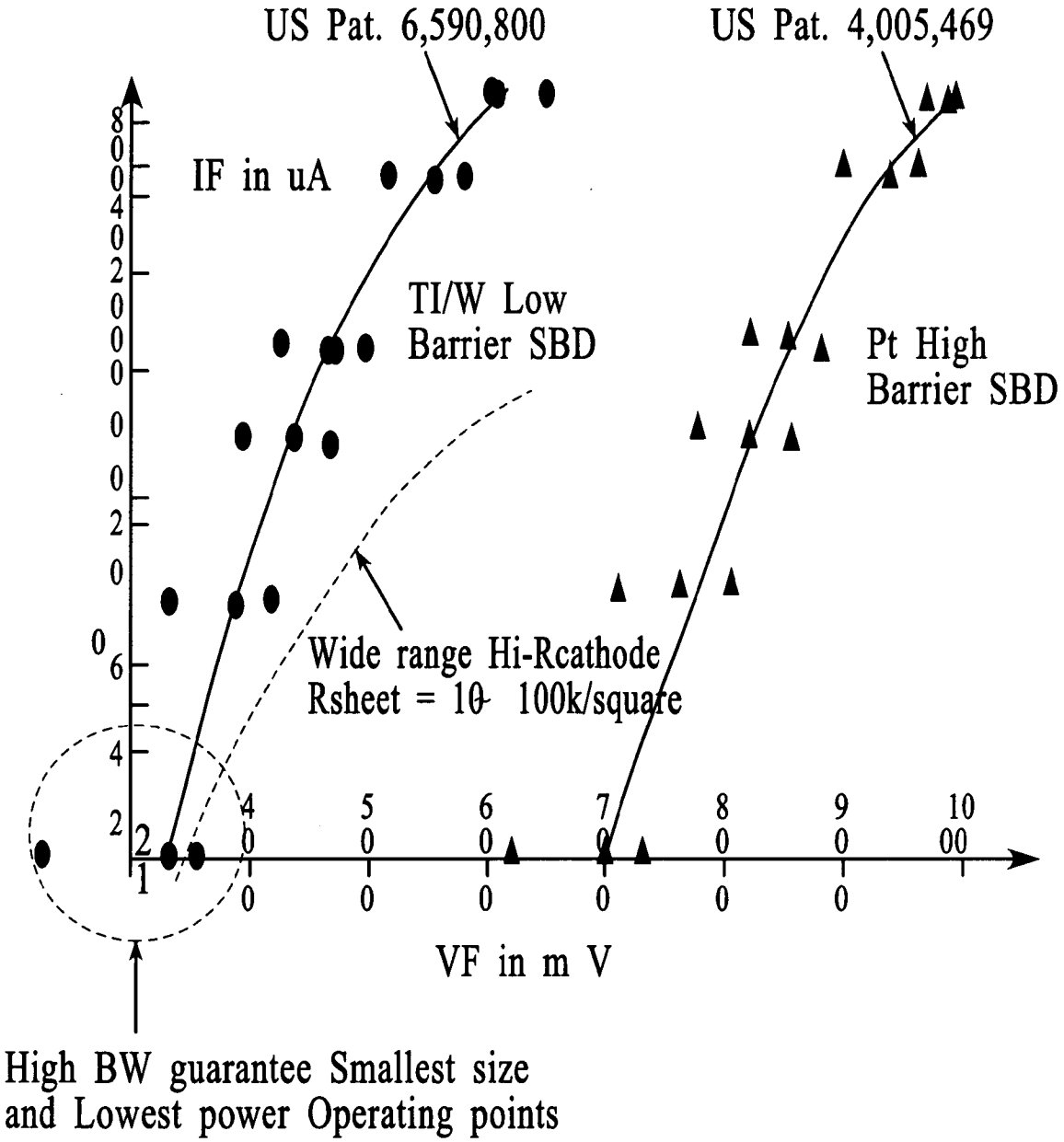
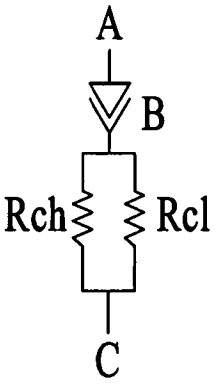
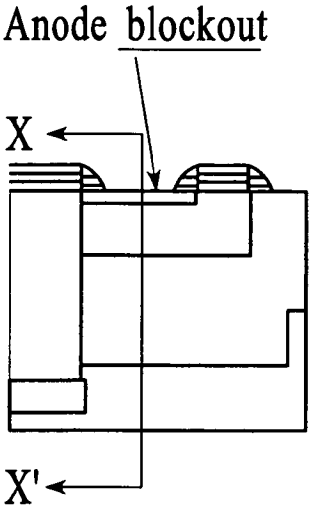
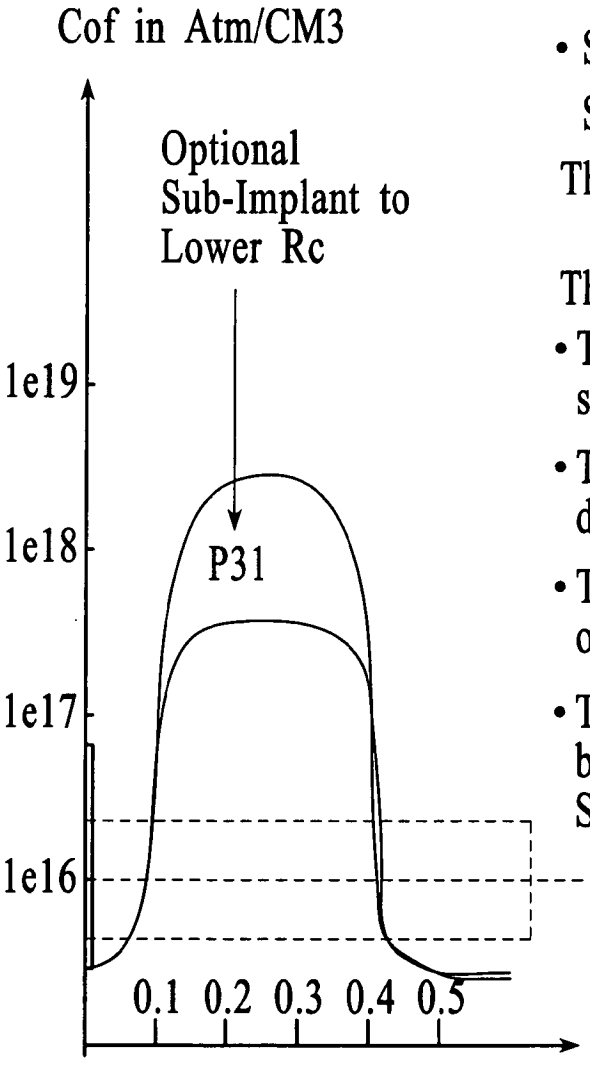


FIG.4

, SBD Rc effect







- SBD Device Structures

The Anode is formed by Metal-Si compound - Ti3Si4

The Cathode has two segments

- Tch is the high sheet rho part- several Kohm/sq
- Tch may be formed by epi or low dosage Implant ~ 10^{16} atm/cm^3
- Tcl is the low sheet rho part <100 ohm/sq
- Tcl may be formed by epi with barried diffusion or high dosage Sub-Implant ~ 10^{16} atm/cm^3

SBD Rc effect 2

The Re effect					
Assumption: W/O sub implant, from Irvin					
Cio alm/cm3		1.00E+15	5.00E+15	1.00E+15	5.00E+15
Rho ohm-cm		4.7	1.1	0.6	0.15
Dio um	0.1	47000	11000	6000	1500
Rsh-Ohm/sq=Rho/Dio	0.2	23500	5500	3000	750
	0.3	15666.667	3666.6667	2000	500

Assumption: With sub implant, Gaussian							
Cio atm/cm3		1.00E+15	5.00E+15	1.00E+16	5.00E+16	1.00E+17	1.00E+18
Sigma 1/ohm-cm	Noc=le15		0.4	0.8	3	5	20
	Noc=le17			0.2	0.8	2	6
Rho ohm-cm	Noc=le15		2.5	1.25	0.333333	0.2	0.05
Rsh Xw um	0.2		12500	6250	1667	1000	250
	0.4		6250	3125	833	500	125
	0.6		4167	2083	556	333	83

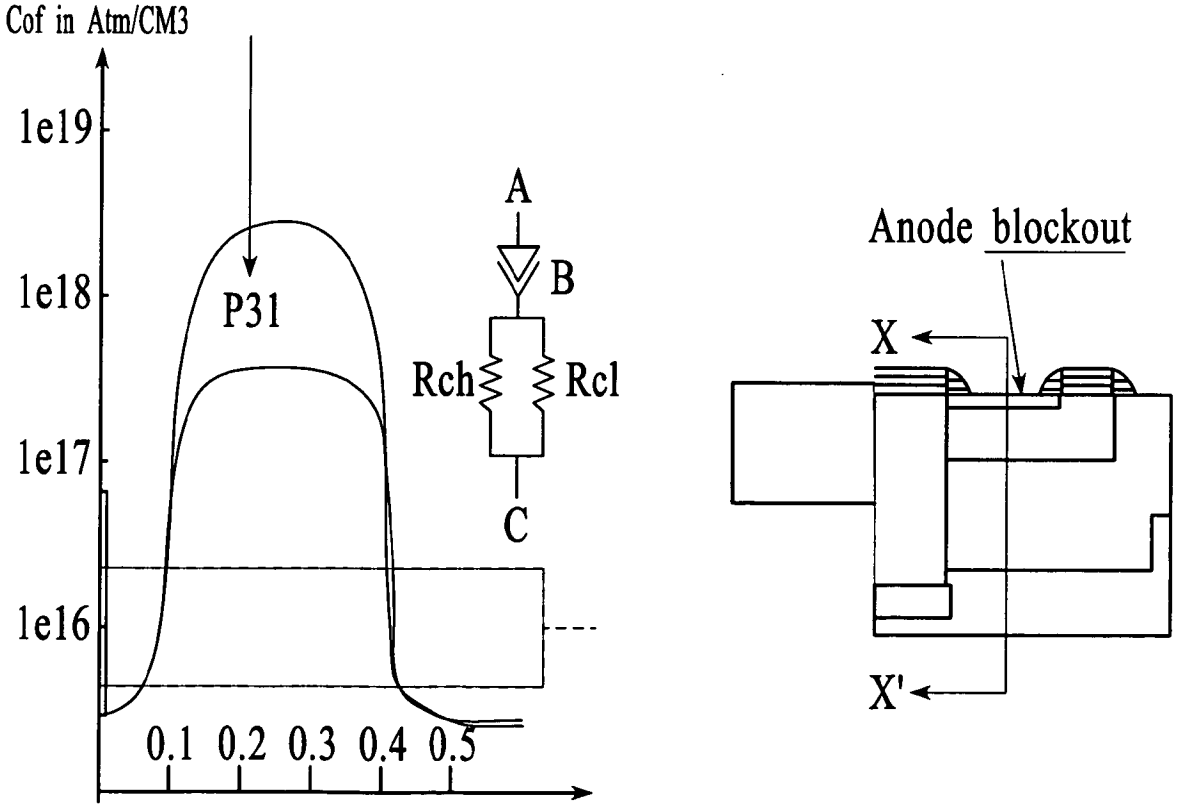


FIG.5

Open Reference literature

Today, advanced wafer packaging processes al Hewlett-Packard to ma low cost surface moun diodes in high volumes marcial and consumer applications. Tradition of these diodes are use ing and power monitor applications such as in cordless phones, satell ston receivers, RFID (r frequency identificatio and many others. How creesing number of the are also used in digital applications such as th of transistor, optocoup erational amplifier circ over-voltage protectio and clamping.

When the Schottky diode is reversed biased, the potential barrier for electrons becomes large: hence there is a small probability that an electron will have sufficient thermal energy to cross the junction. The reverse leakage current will be in the nanoampere range.

In contrast to a conventional p-n junction, current in the Schottky diode is carried only by majority carriers. Because no minority carrier charge storage effects are present, Schottky diodes have carrier lifetimes of less than 100 ps and are extremely fast switching semiconductors.

Another significant diffe tween Schottky and p-n voltage drop des have a t .3 V compar unction diod

careful man er of the Sc che choice o the n-dope aracteristic on capacita es resistanc oltage Vbr a

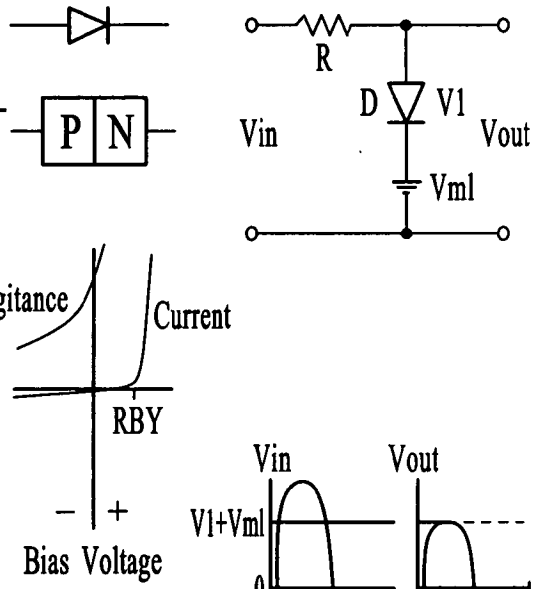
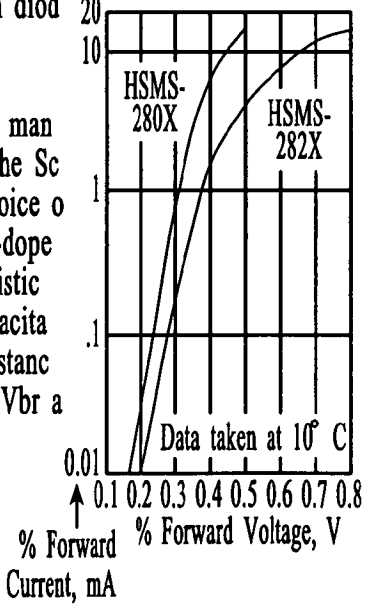


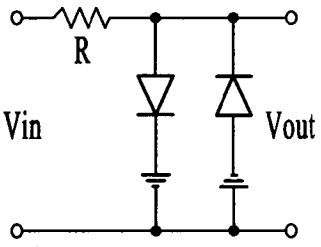
Figure 4.

Table 1.

Parameter	HSMS-280X	HSMS-282X
Cjo	1.5	0.7
Vbr	75	0
Rc	30	5
Ec	0.69	0.69
Iuv	10.0E-6	10.0E-4
Is	3.0E-8	3.0E-8
N	1.08	1.08
Pe	0.65	0.65
Pr	2	2
M	0.5	0.5

Figure 2. Forward Current vs. Forward Voltage





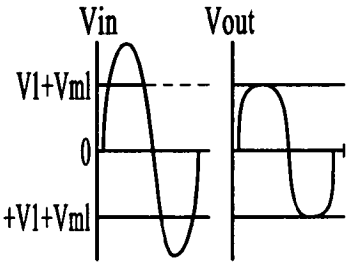


Figure 4.

FIG.6A

Reference literature

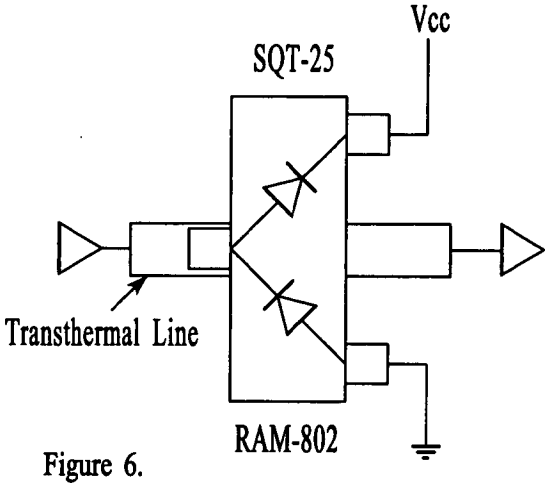


Figure 6.

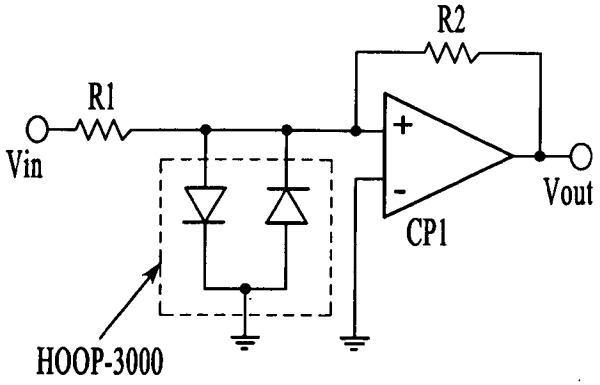


Figure 7.

Protection and Improving Performance of Operational Amplifiers

Operational amplifier input overload, which can occur in the form of excessive common-mode or differential voltages, can result in a voltage breakdown that will damage or destroy the input transistors of the device.

Amplifier Protection

Protection of an operational amplifier from high input voltages can be achieved by using a series diode (HSMS-28X2) as shown in Figure 7. The diodes limit the voltages at the input to the operational amplifier to safe levels (approx. 0.4 V) without restricting the signal swing.

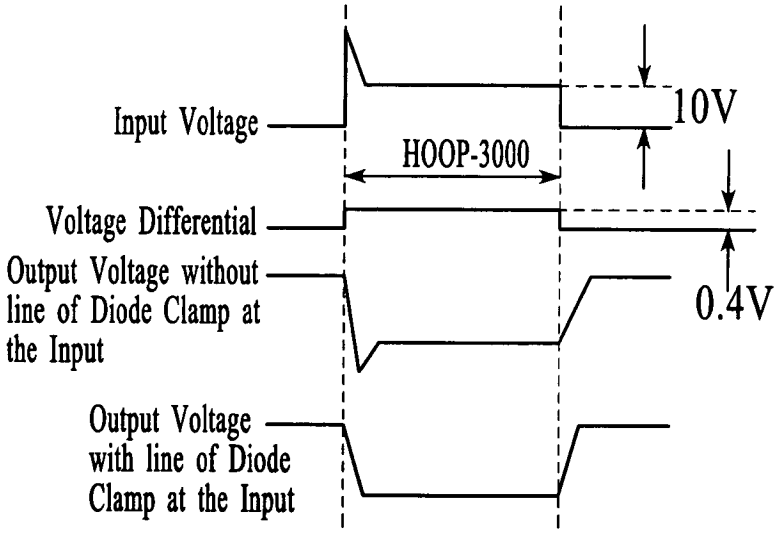


Figure 8.

Settling Time-Speedup

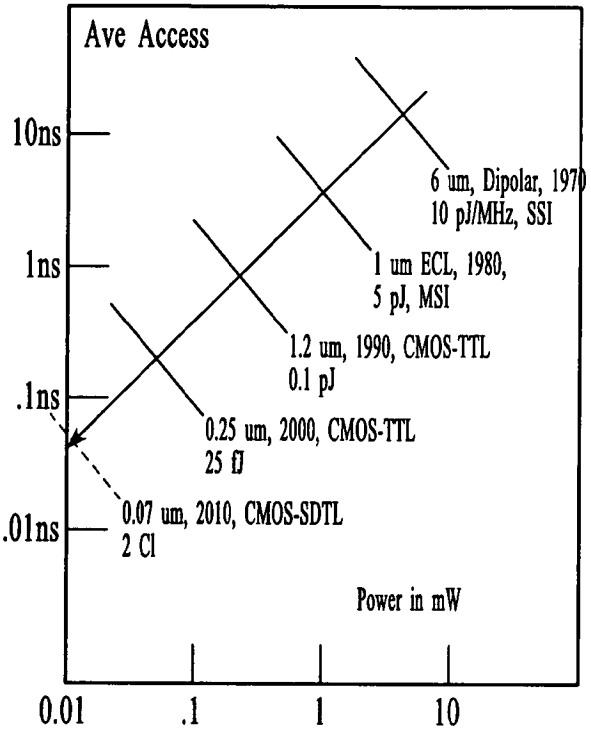
An important consideration for operational amplifier performance age, V3 - V2. Since the integration circuit typically has a slow responce time, it cannot respond to fast input spikes, thus resulting in ringing in the output signal and cellent choice for a variety of non-RB allpications. For further information, contact your local Hewlett-Packard sales office.

FIG.6B

5th Gen. IC, Schottky-CMOS-Logic (SCL™)

IC circuit solution and cost trends
Figure of merit index comparison on NAND4 gate

	Area	Access time	Power	Defect	AAP Cost
Bipolar TTL	100	100	100	100	1E8
Bipolar SCL 1985	200	10	200	200	8E7
CMOS TTL 2000	10	10	10	10	1E4
CMOS-SDTL 2004	2	2	2	2	16
	Bipolar			CMOS	
Tech rules/pacs	1970	1980	1990	2000	2010
GoVWb Ang	4000	2000	200	70	50
H um left	6	3	1	0.25	0.07
H um tibs	1	0.5	0.4	0.3	0.2
Contact/space um	10	2	1.2	0.25	0.2
Typ C load in F	10pF	1pF	0.4pF	200fF	50fF
Op. V volt	8	5	3.3	2.5	1.2
Op. 1 out CV*f	1	0.1	.01	1uA	10uA
Speed nb	70	10	3	500 pS	200 pS
Power*Speed pl	560	5	0.1	0.03	1.3 Cl
Vc inch	3.5	4	6	8	12
Density Gaus	100	2000	20k	200k	1M



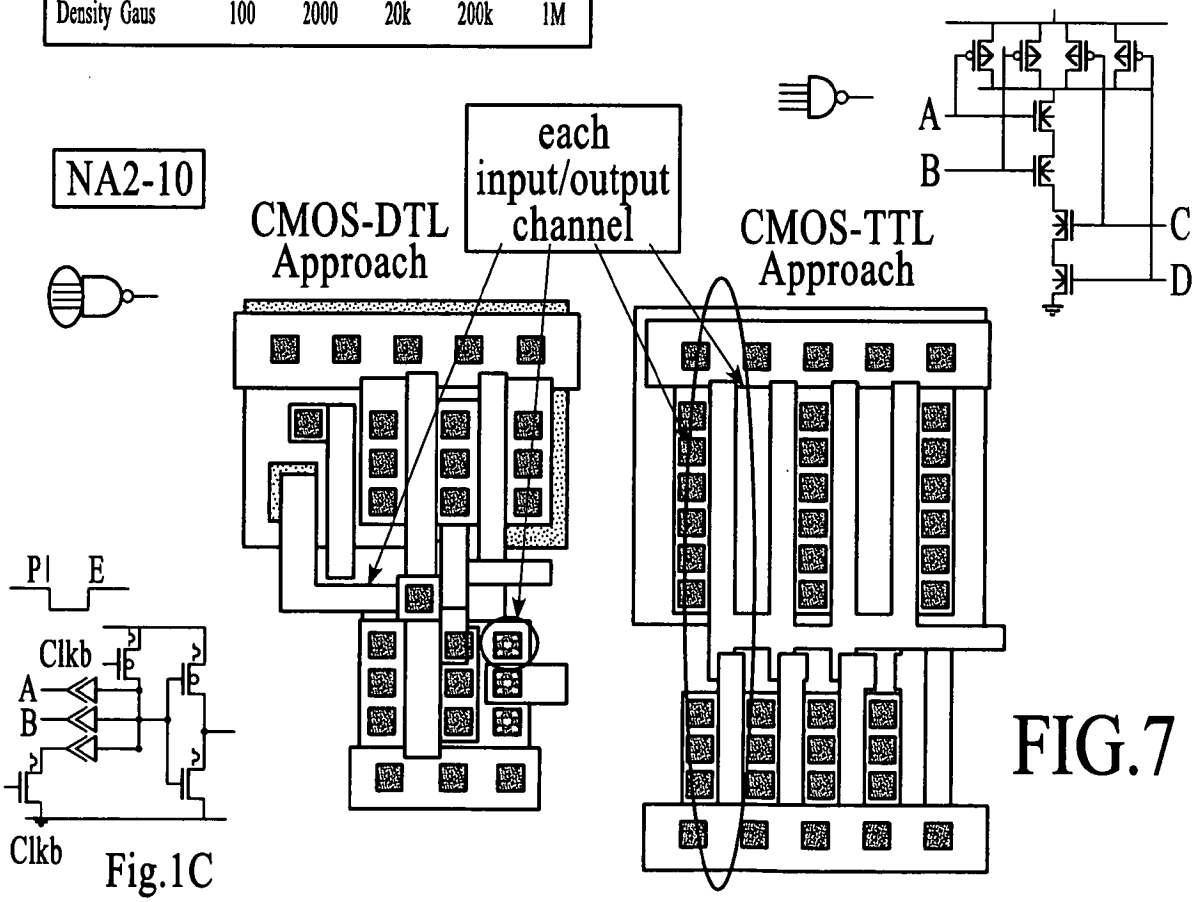


Fig.1C

FIG.7

Demonstrative
Embedded Library Solutions

Exemplary logic applications additional to MLC arrays

Low power IO Block functions

- ESD clamp diodes and line terminators
- Schmitt trigger at 1.2V
- ZBUF 1.2V
- Transceivers 1.2V

Low power internal logic and level shifter

- Inverter, NAND, NOR, DFF, and combinationals,
- XOR4
- Anolog Differential Sense Amp and latch 1, 2

Special functions

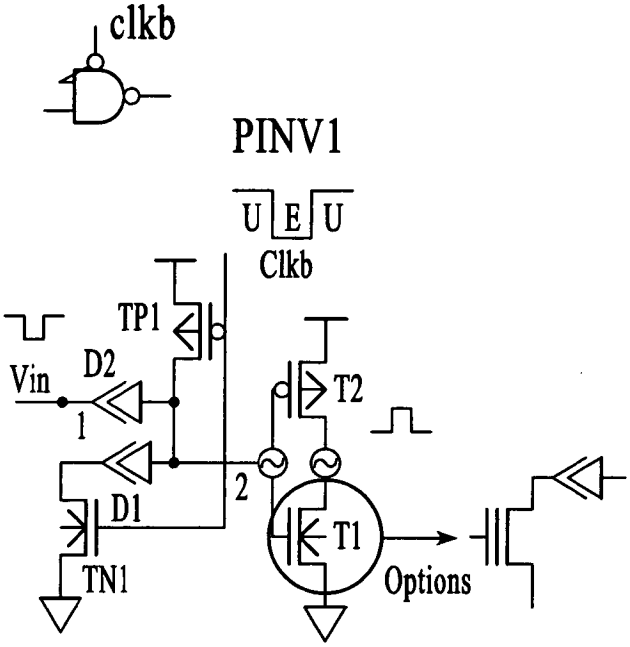
1. Oscillators
2. PLL and DLL
3. High speed RAM
4. Mask ROM, OTP and FPGA
5. Arithmetic; Adder + Multiplier
6. Absolute value function
7. ADC/DAC

Controller Applications

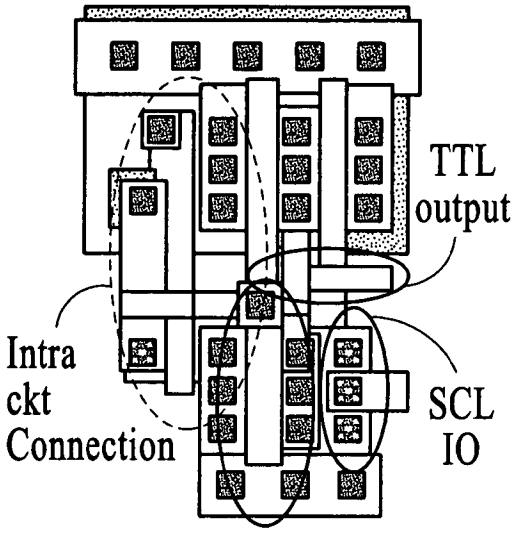
- Semiconductor Disks
- Image strorage and access devices
- Network storage and access devices
- Wireless and mobile communications
- Multimedia interfaces and data transports
- Generic Programmable computing devices

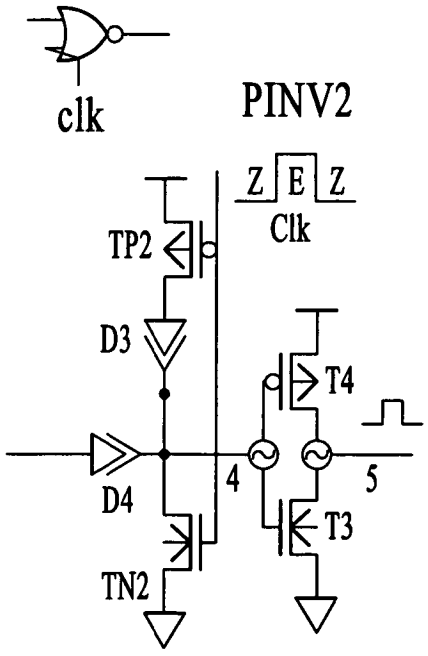
FIG.8

Pulsed INV



Vin	Clkb	Vo
X	H	H
1	L	0
0	L	1





Vin	Clk	Vo
X	L	L
1	H	0
0	H	1

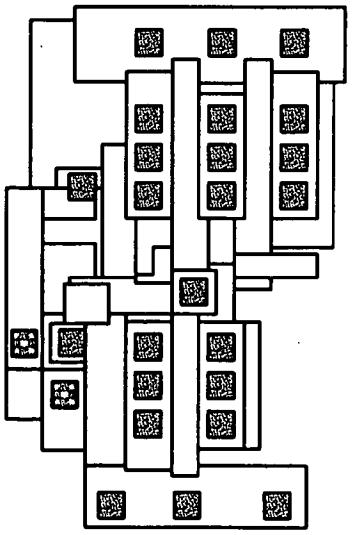


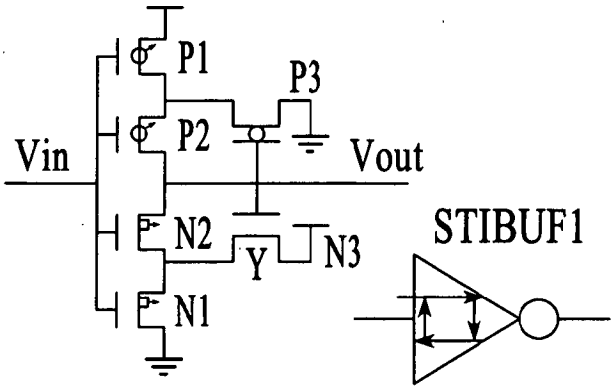
FIG.9

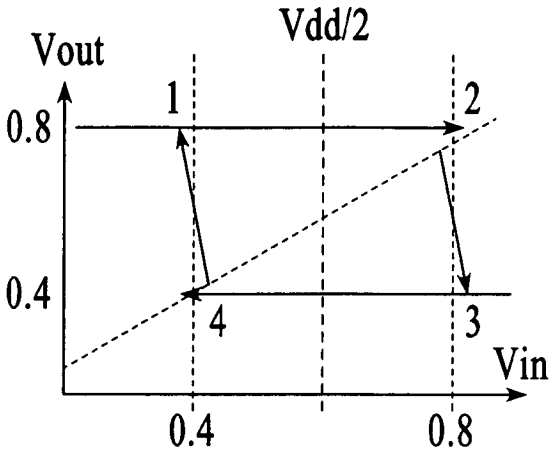
Lo Power STIBUF

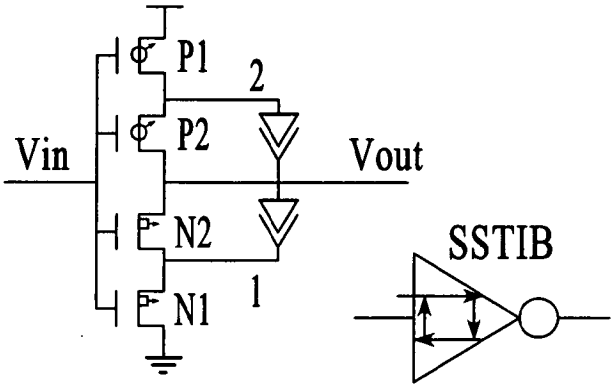
Schmitt Trigger- for VDD=1.2-1.5V, Different Input Vt

*VtLH=0.8V

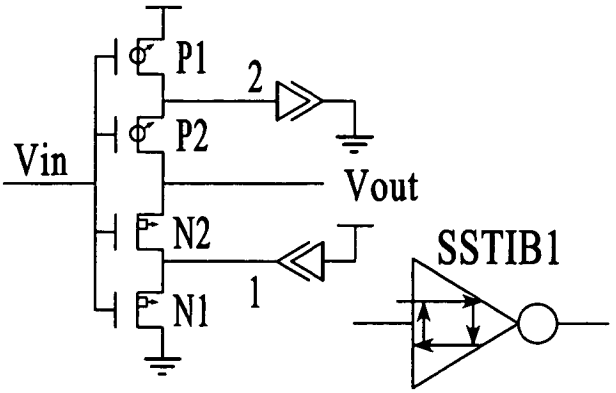
*VtHL=0.4V







*	Vin	V1	V2	Vout
1.	0	1.2	1.5	1.5
2.	0.4	1.2	1.5	1.5
3.	0.6	1.2	1.5	1.5
4.	0.8	0.5	1.1	0.8
5.	1.2	0	0.3	0
6.	1.5	0	0	0
7.	1.2	0	0.3	0
8.	0.8	0.5	1.1	0.8
9.	0.4	1.2	1.5	1.5
10.	0	1.2	1.5	1.5



*	Vin	V1	V2	Vout
1.	0	1.2	1.5	1.5
2.	0.4	1.2	1.5	1.5
3.	0.6	1.2	1.5	1.5
4.	0.8	0.5	1.1	0.8
5.	1.2	0	0	0
6.	1.5	0	0	0
7.	1.2	0	0	0
8.	0.8	0	1.0	1.3
9.	0.4	1.2	1.5	1.5
10.	0	1.2	1.5	1.5

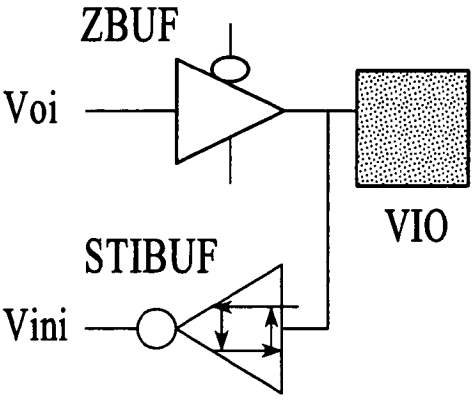
FIG.10

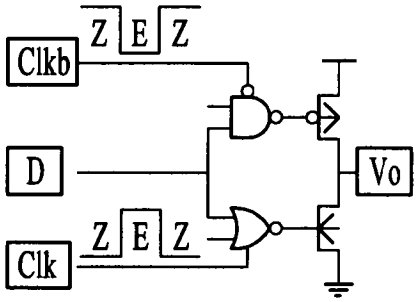
Lo Power SIOIBUF

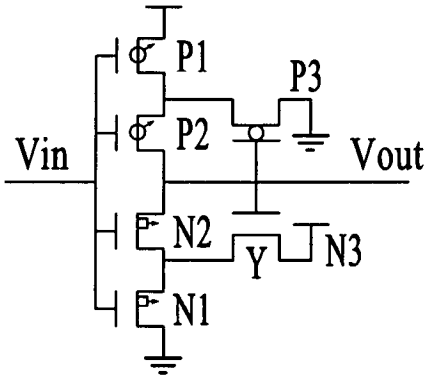
Single Phase Schmitt Trigger-
VDD=1.2-1.5V
Different Input Vt
* VtLH=0.8V
* VtHL=0.4V

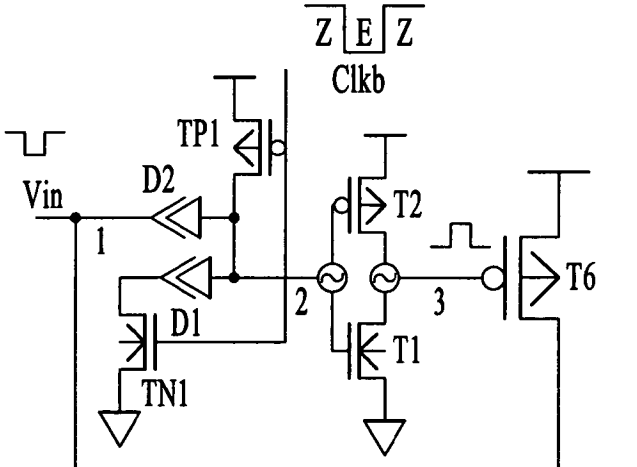
ZBUF

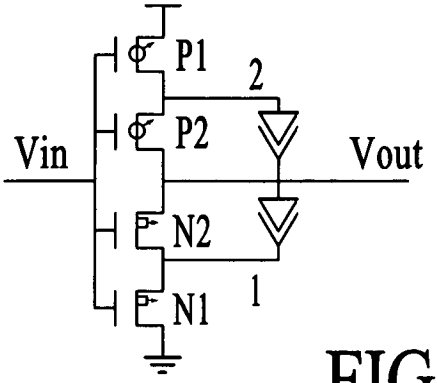
1. Complementary clock
2. Can add predriver stages for large output Transistors
3. 50 ohm double terminated lines
4. Vtm = 0.6V











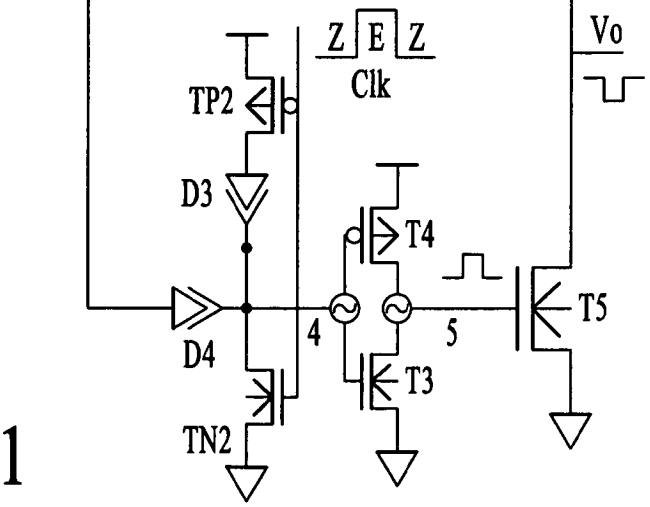
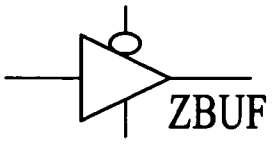
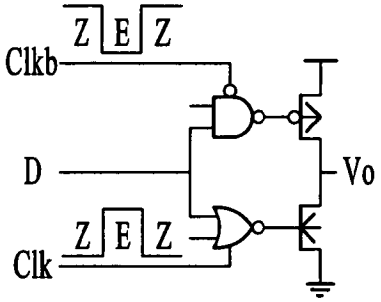


FIG.11

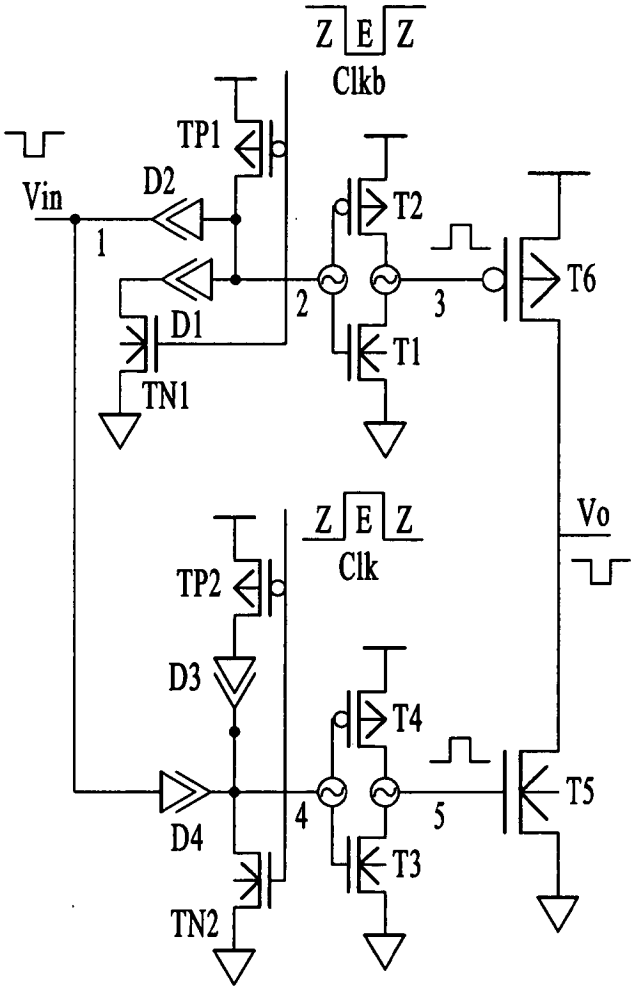
ZBUF & Transceiver4 -SCL



Vin	Clk	Clkb	Vo
X	L	H	Z
1	H	L	1
0	H	L	0



Clk and Clkb are complimentary pairs
T1, T2 can scale up 3 stages to drive T6
T3, T4 can scale up 3 stages to drive T5



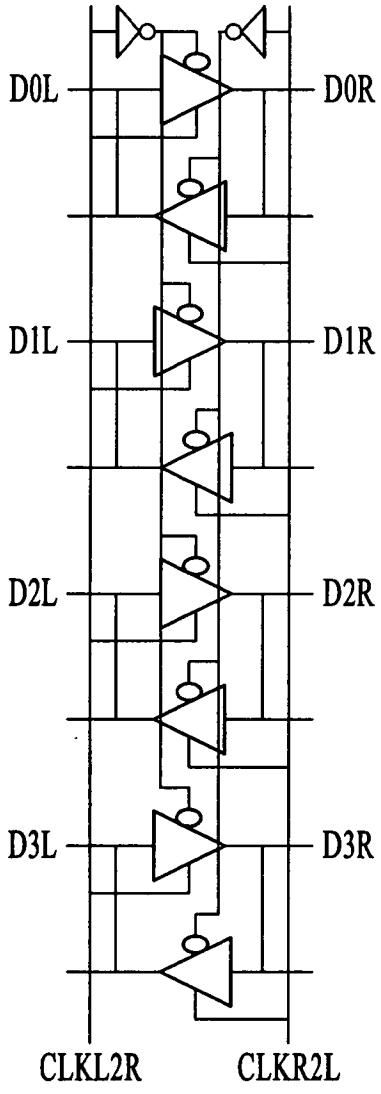


FIG.12

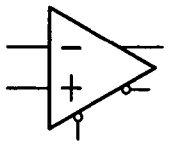
Hi Power GTLOBUF, Lo Power PDIBUF

GTL-OBUF

- Vcc = 1.2V
- Vtm = 0.6V, Rtm = 25 ohm
- Voh = 0.8V
- Vol = 0.4V

Pulsed DIFF IBUF

- Neg. CLKB
- DIFF input ~ 0.6v
- Single/Dual phase In/Output



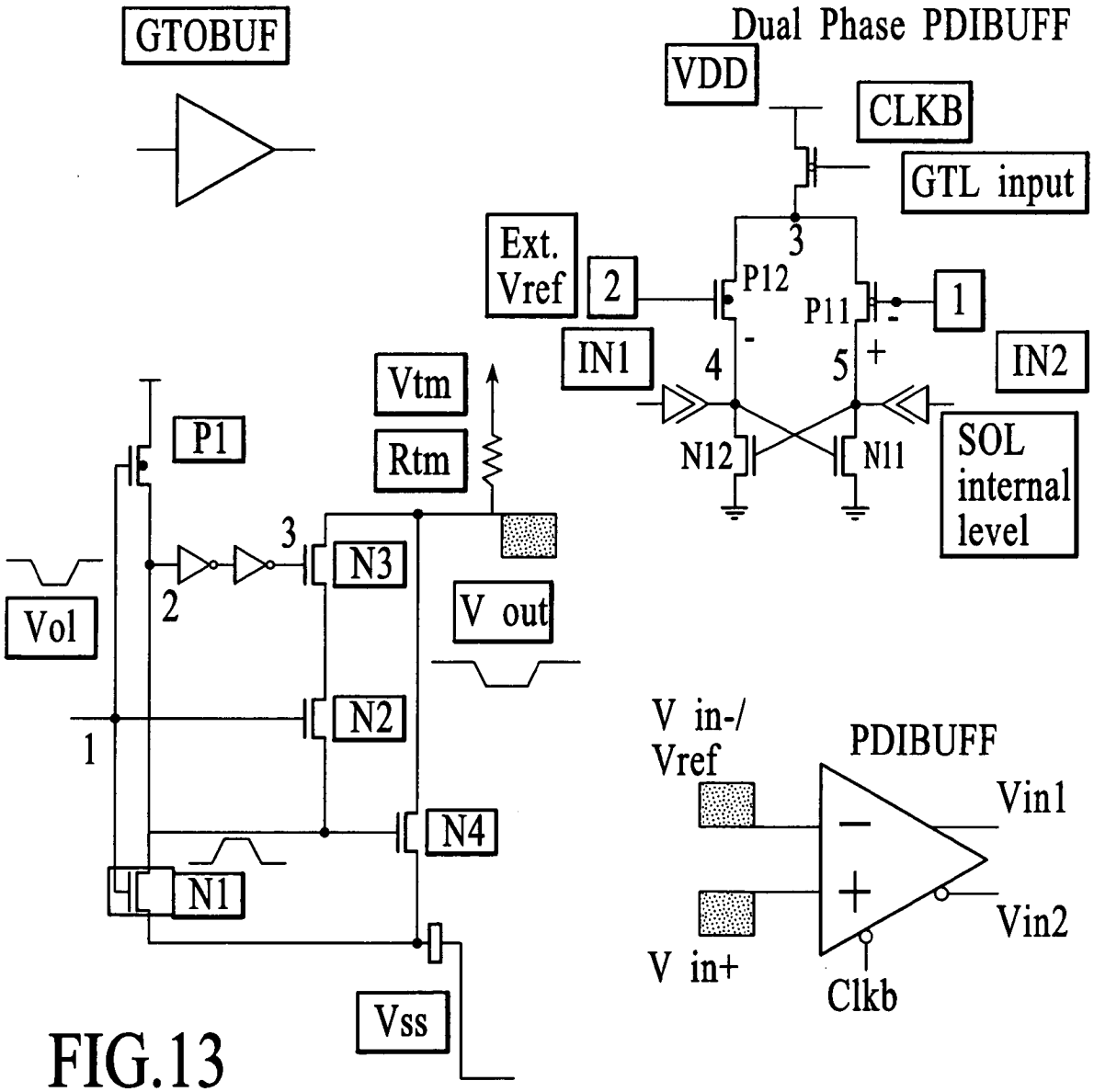


FIG.13

CMOS-TTL

XOR2: W/O BUF

Transistor: 3 NTX 3PTX

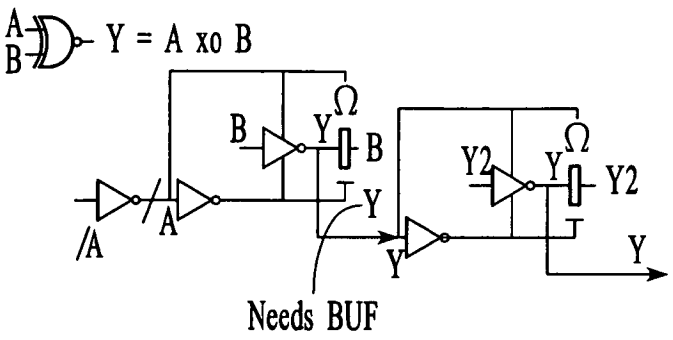
Area/load units: 3 6

Tacc: 2x (50:70:100),

-150ps

effects: Pre-dvr, current,

loading



XOR4: W/O BUF

Transistor: 9 NTX 18PTX

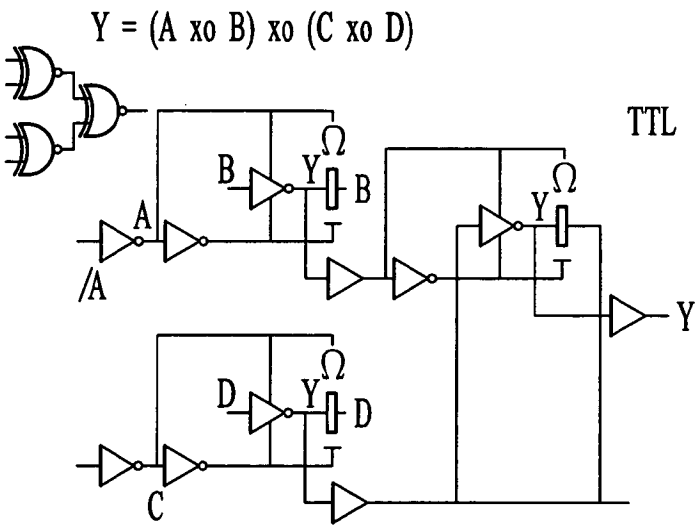
27

Tacc: 3x (50:70:250),

>800ps

effects: Pre-dvr, current,

loading



XOR4: W/O BUF

Transistor: 17 NTX 24PTX

41

Tacc: 3x (70:120:170),

>400ps

effects: Pre-dvr, current,

loading

GSD

CMOS-DTL

XOR4: Built-in BUF

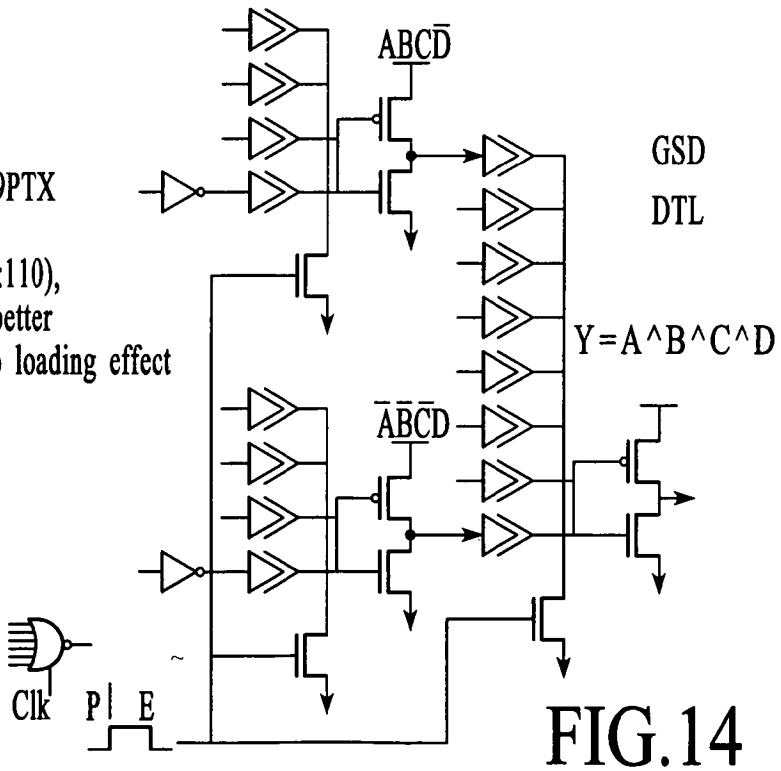
Transistor: 18 NTX 9PTX

27

Tacc: 2x (50:80:110),

<200ps 4 times better

effects: No ripple, No loading effect



Applications:

Packet switching: Preamble data stream check

Parity tree

Address change detection

Multi-phase PLL clock

FIG.14

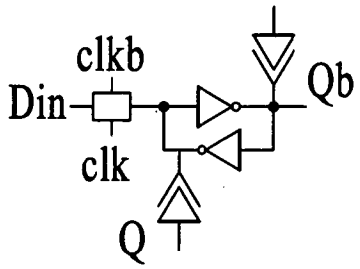
Dlatch, Osc

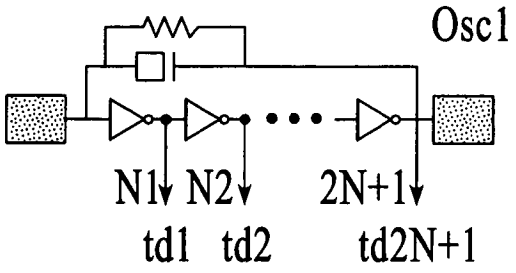
Multivalued outputs

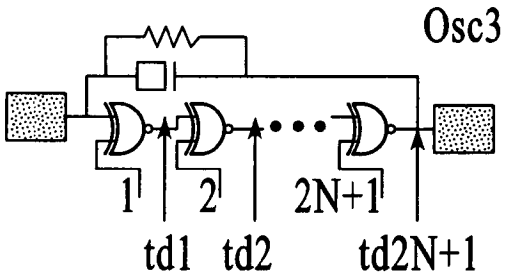
- CMOS level
- CML level

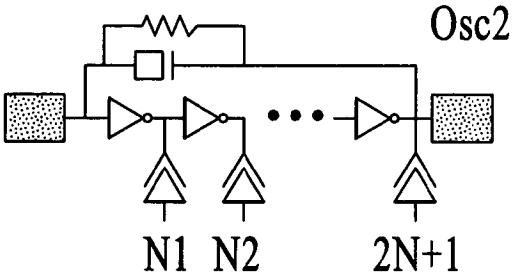
CMOS Osc.: 2 Types

- SCL Oscillator/Delay taps
- Osc.: 2 types









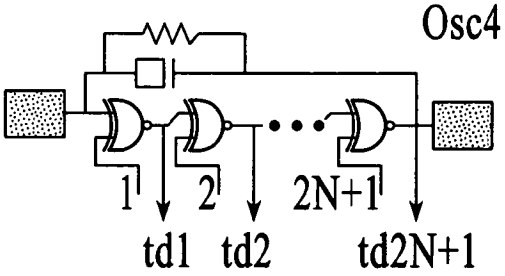
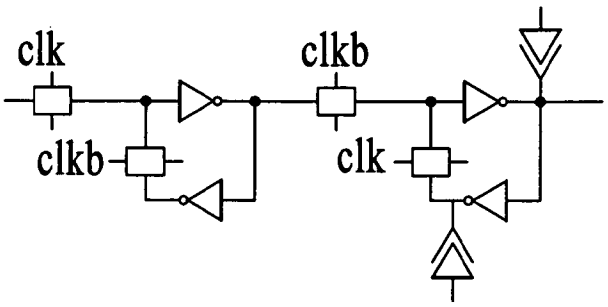
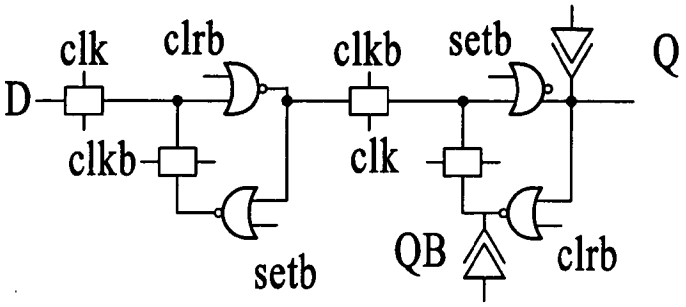


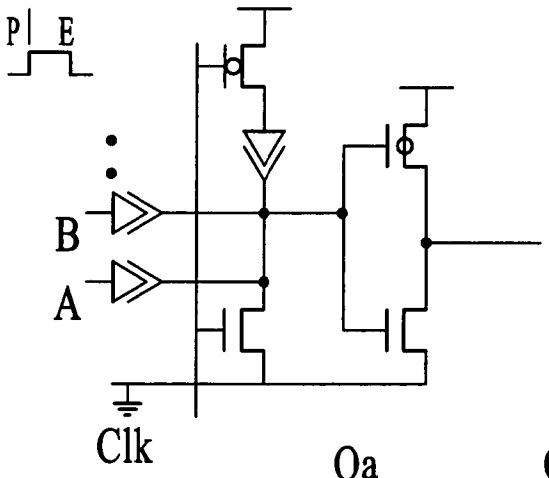
FIG.15

GDFF-SCL



- Static DFF
- Set/Reset DFF
- SCAN register element





- Serial IN Parallel Out Shift Reg. - SIPOSR

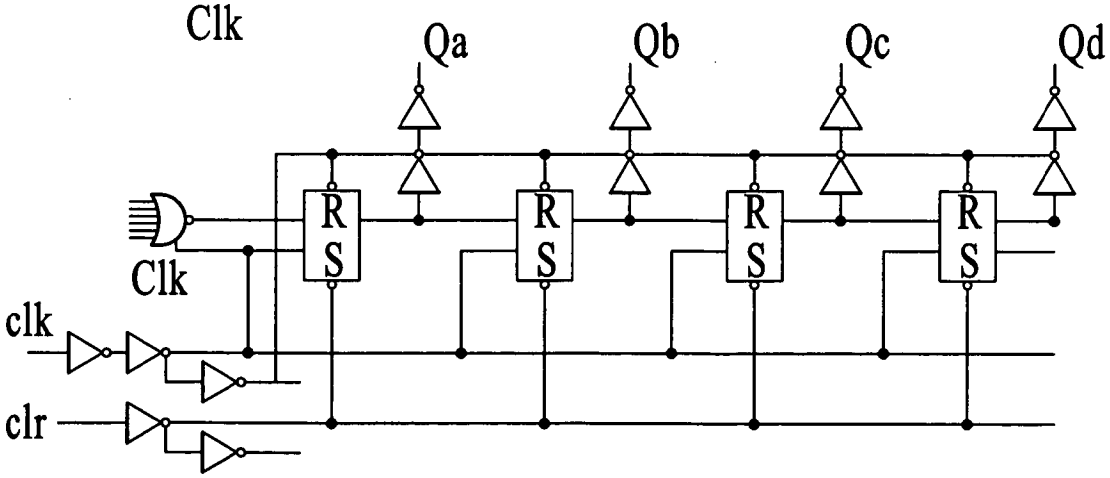
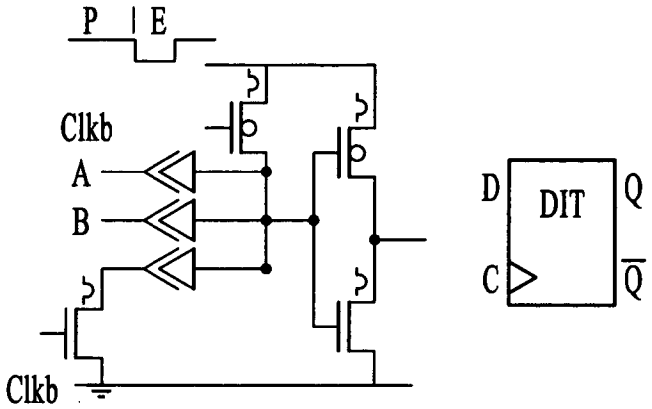


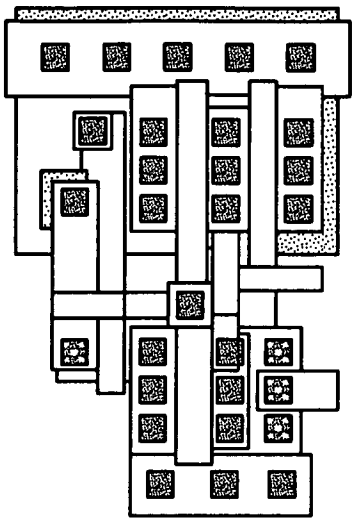
FIG.16

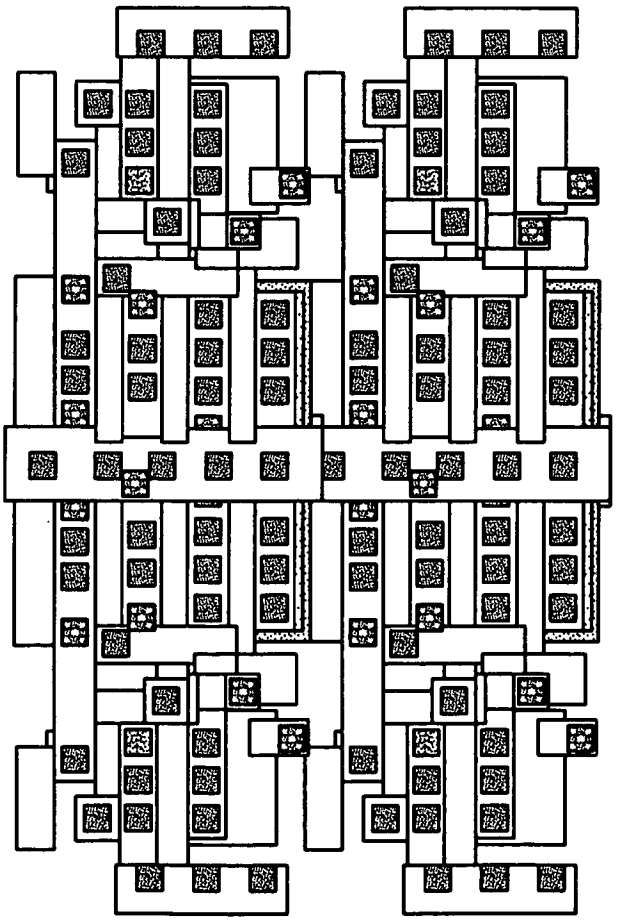
DFF with GNAND

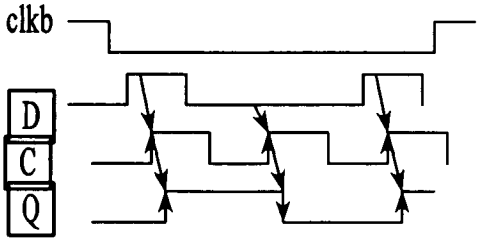
- GNAND Approach
- 18 Smaller Transistors

- CMOS TTL, 22txs
- 2 phase clock
- Slow serial pass Tx
- Scanable









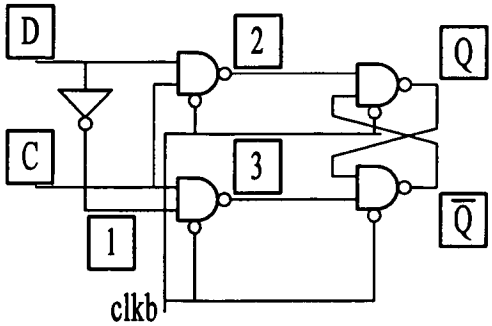
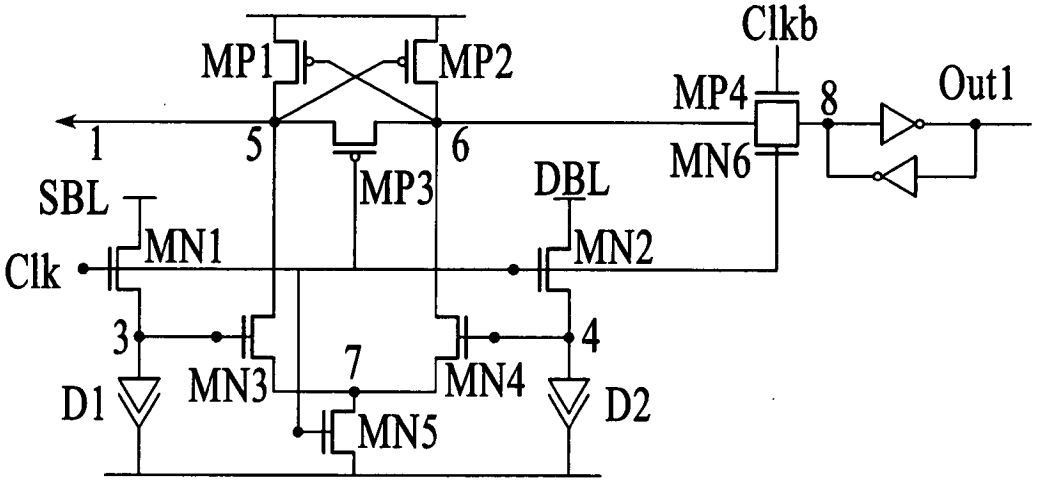


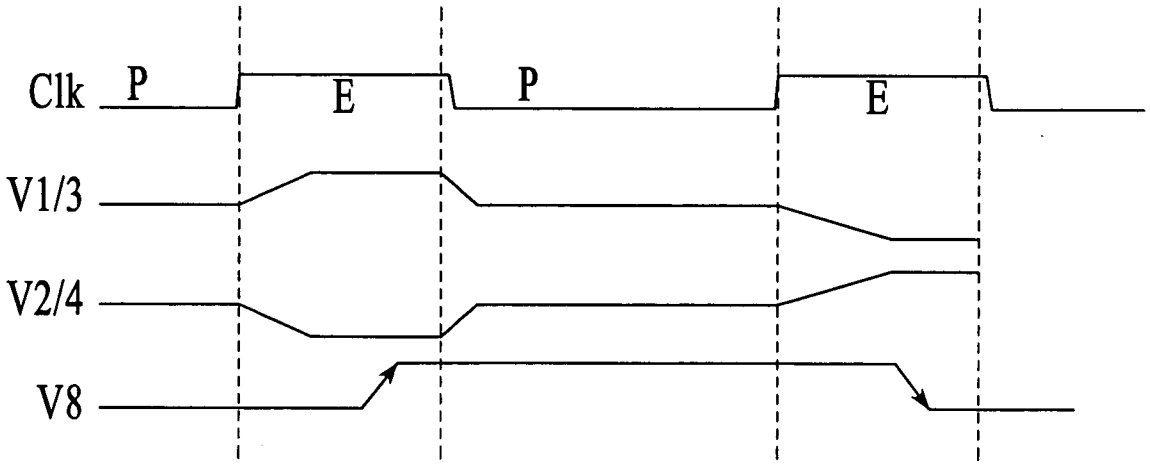
FIG.17

IOBUF/Sense Latch

Dual Phase Dynamic Sense Amp

- Hi Embedded Resistance with D1, D2
- Diff Inputs may be V3, V4
- Diff Inputs may be V2, V2





Sense Amp Operation

Precharge: D1, D2 clamp MN3,4,5 OFF.

Evaluate: V3,4 pulsed on>>MN3,4,5 turned on>>MP1,2,3

Latching>>Output Latch reset

FIG.18

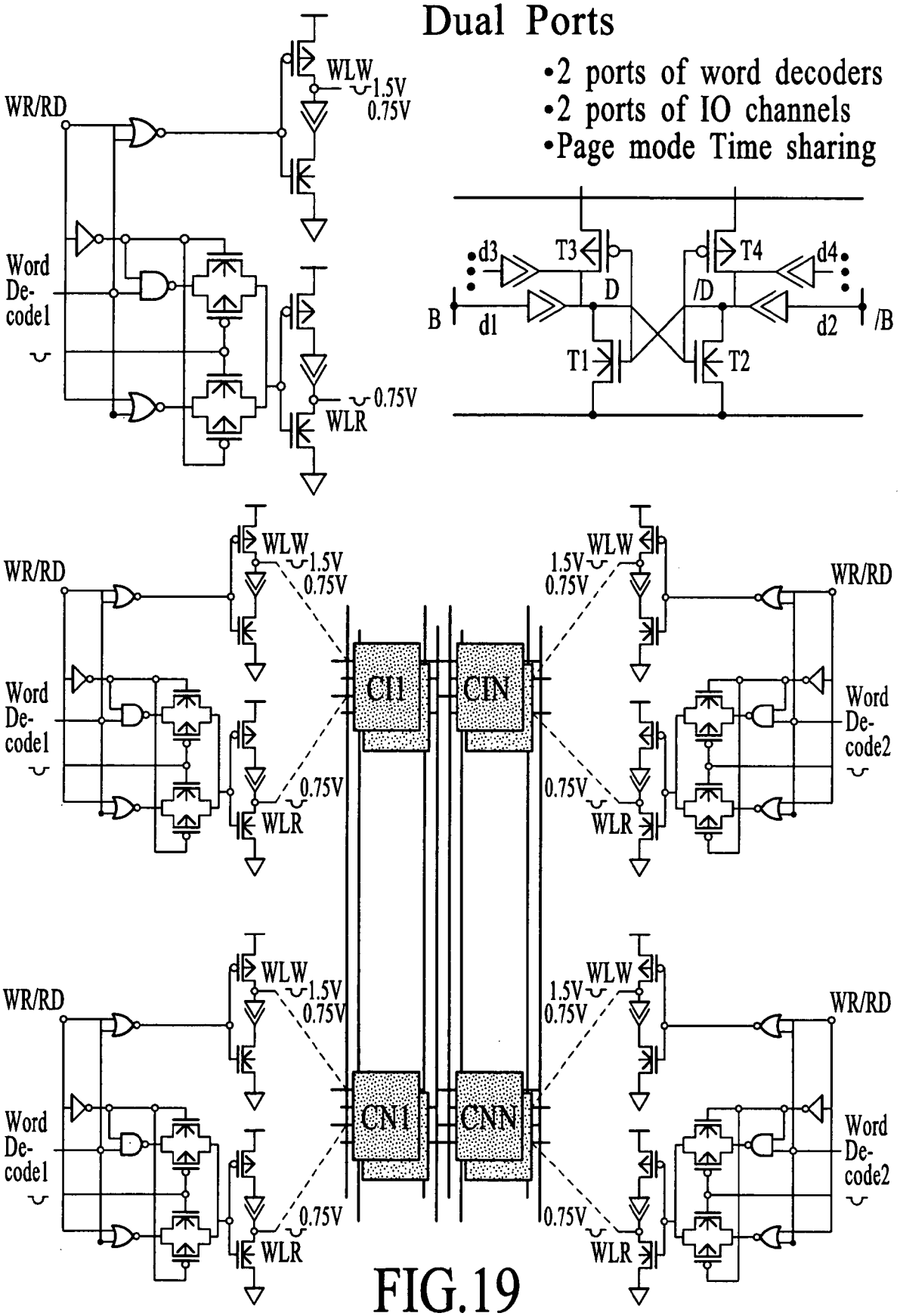
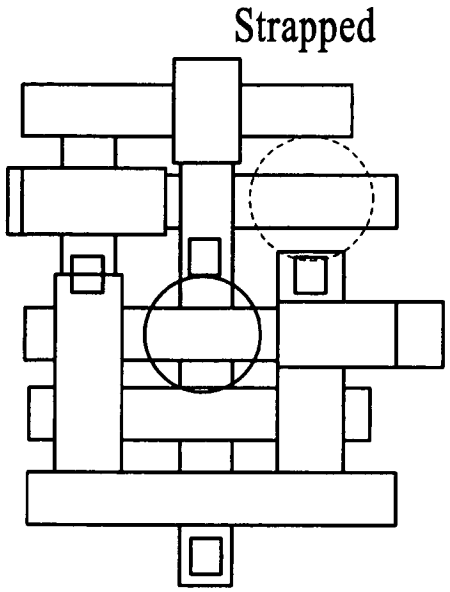


FIG.19

Dynamic Read Only Memory-Hard and FPGA

DSP-Translation Lookoxide Buf for coefficients
Controller-Microcode instructions
Tx Array: Dif Poly Defined
- Common Gnd
- Shared Drain Contact
- Strapped MZ WL
- Pre-charged M1 SL

Schottky array-Double density, low cost, high speed
- Vertical SBD, buried N+ cathode lines, with strapped M2 option.
- Pulsed decoder, M1 Word time1, No Poly



Conventional CMOS Transistor ROM

FIG.20A

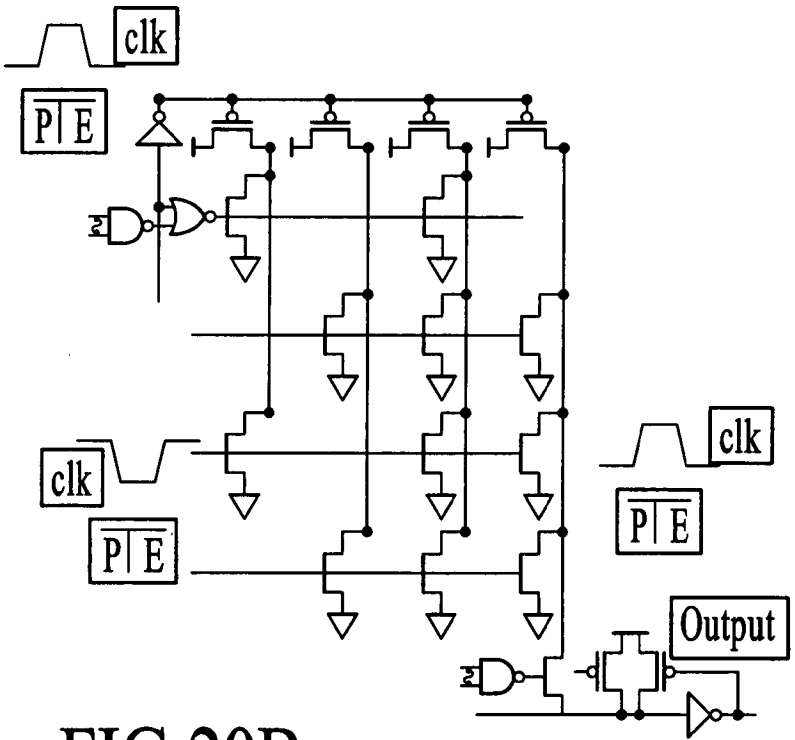


FIG.20B

Dynamic Read Only Memory-Hard and FPGA

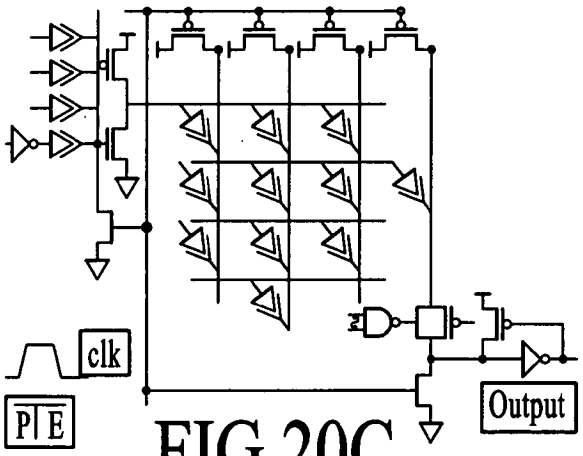


FIG.20C

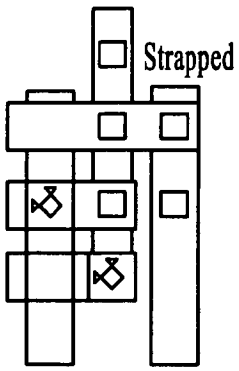


FIG.20D

SCL Dynamic SBD
ROM-Double Density
Faster Access times
Mask prog.

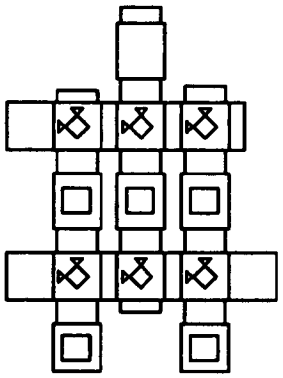


FIG.20E

Legend

LI film	1st Metal Plug
Poly contact	Barrier metal
Polycide	N- cathode region
1st Metal	N+ cathode region
	SiO2

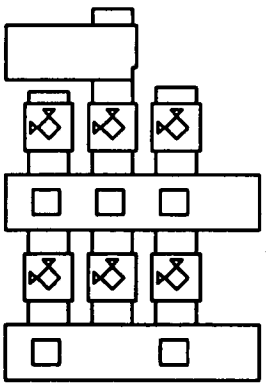


FIG.20F

SCL Dynamic SBD
ROM-Double Density
Faster Access times
Field prog.

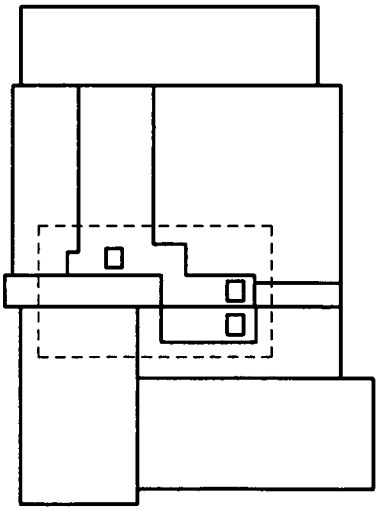


FIG.20G

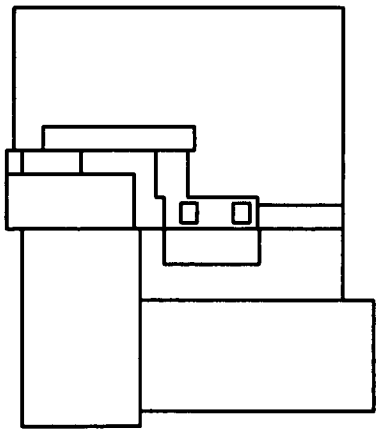


FIG.20H

Two schemes to make fuses of Local Interconnect

ESD Input protection with SBD

Input protection circuits

- High lead-in poly resistors > 100 kohm
- Limit current peaks > p[eaks to < 50 mA
- Conductive SBD and bipolar PN parasitics
- Low Cin < 1-3 pF

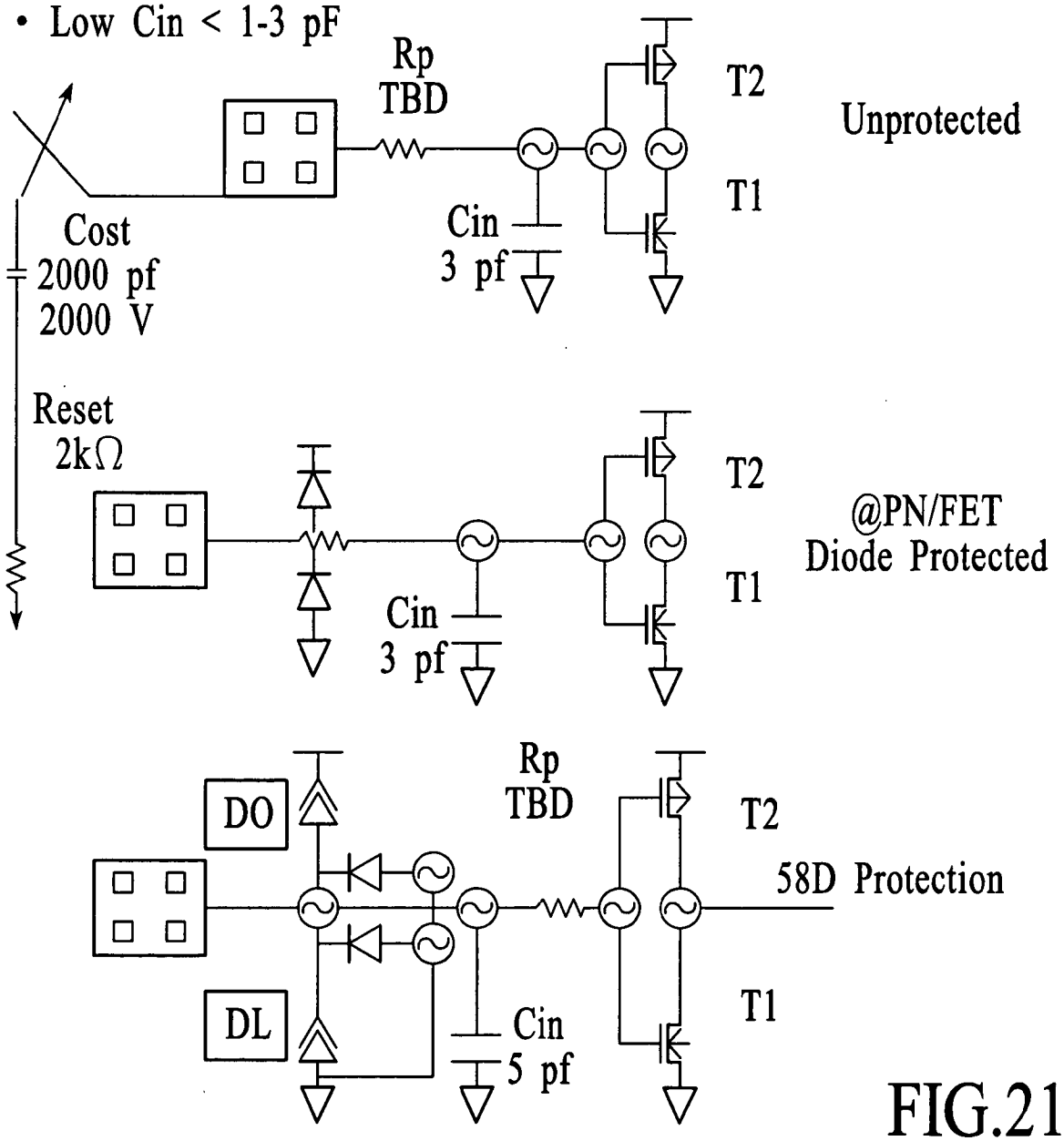
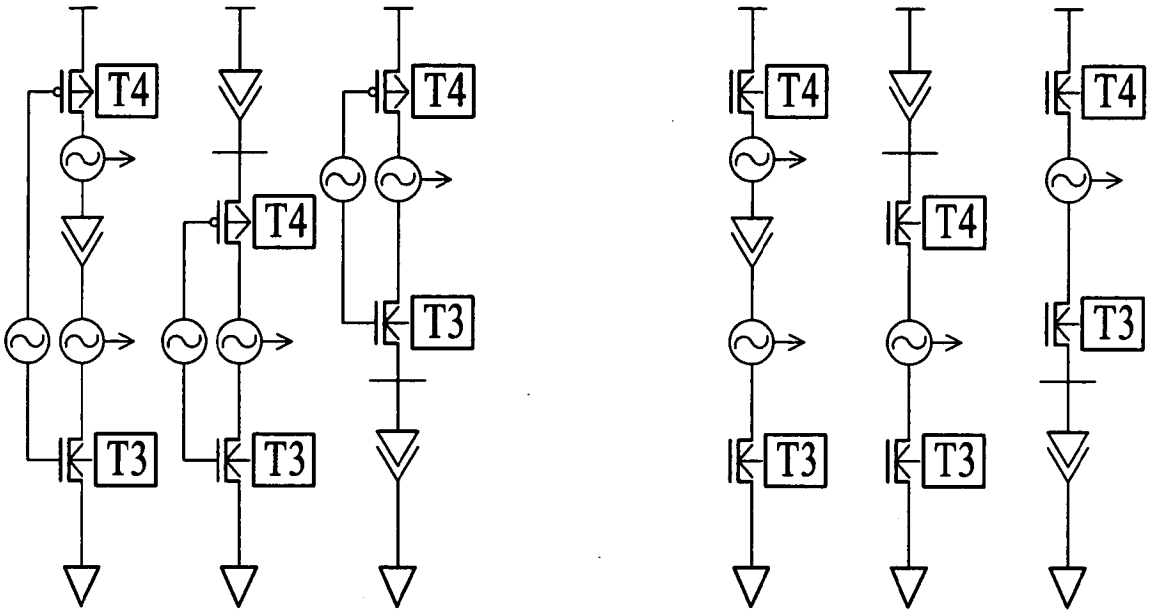


FIG.21

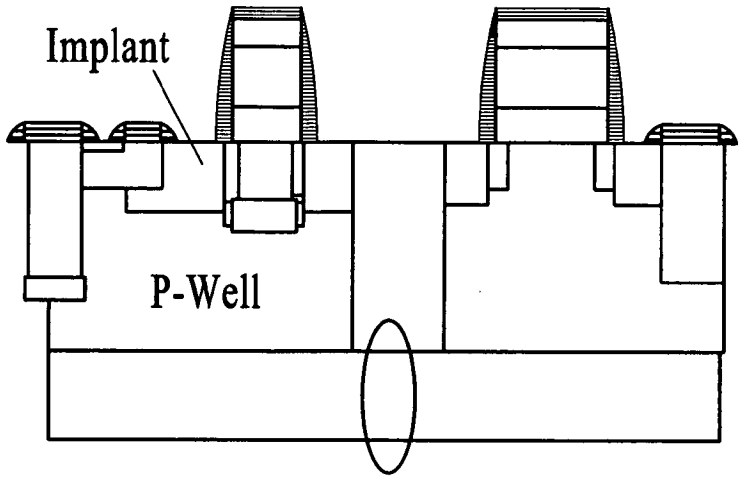


Totem pole level shifting and Vref schemes with SBD string

FIG.22

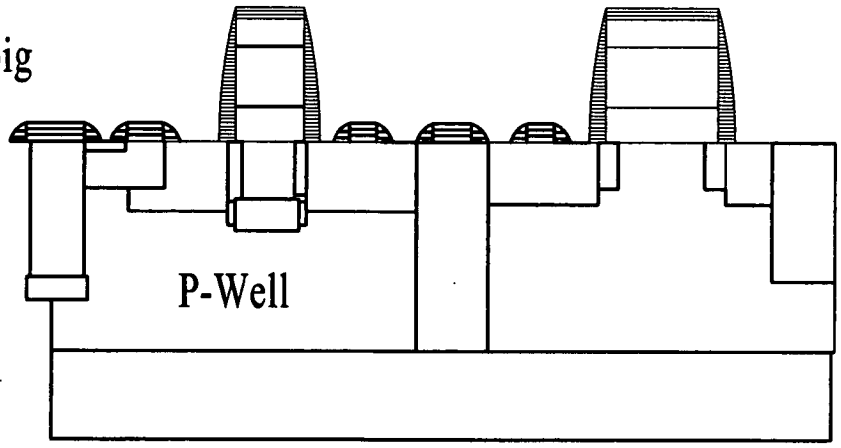
Unprotected and protected P/Nwells

- Area of impact
  - IO cells
  - Array array: logic and Flash beds
- Parasitic device model
  - NPN in Pwell and PNP in Nwell
- Latch up due to lateral PN/PN actions
- Suppression by passive N/Pwell tapping
  - Double ring big areas,
  - less margin
- Suppression by active device tapping
  - Suppress NPN by SBD in NMOS bed-biasing to GND
  - Suppress PNP by SBD in PMOS bed-biasing to VCC



Parasite PN/PN latch-up sweet model of the unprotected CFBT transcievers

FIG.23A



add local active low barrier SBDs as needed

FIG.23B

Input Protection Circuits

Latch up protection, Fig.22C

- Wire SBD in Nwell bed to VCC
- Wire SBD in Pwell bed to GND

Controlled Hot well biasing by SBD, Fig. 23

- Lower Vt

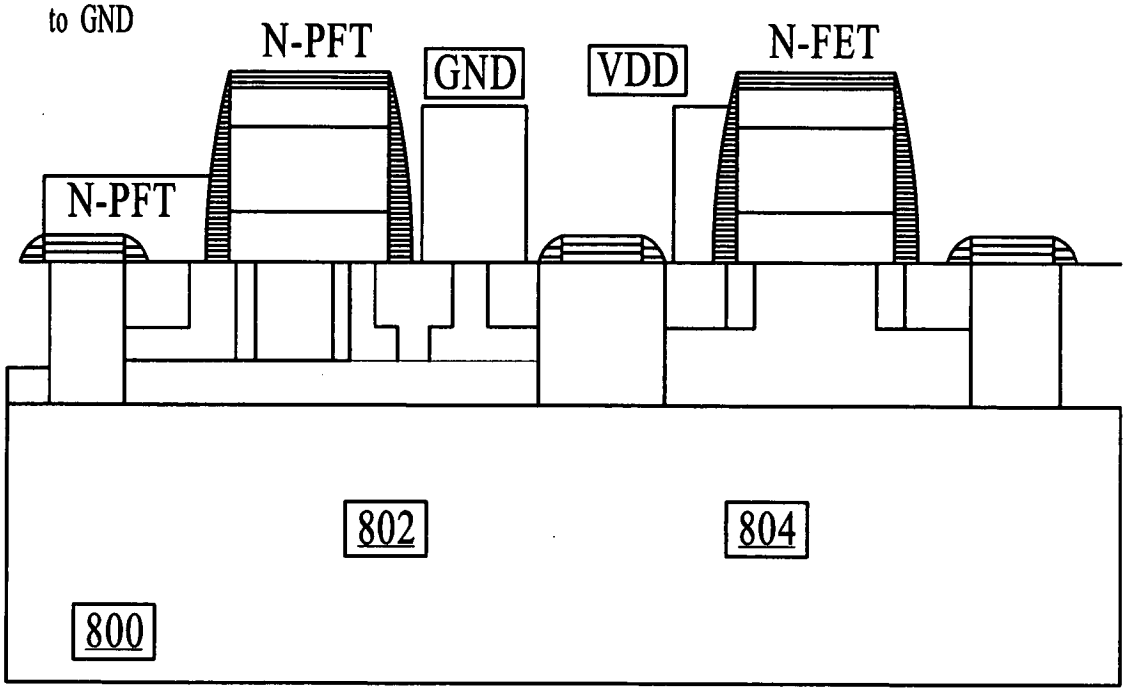


FIG.23C

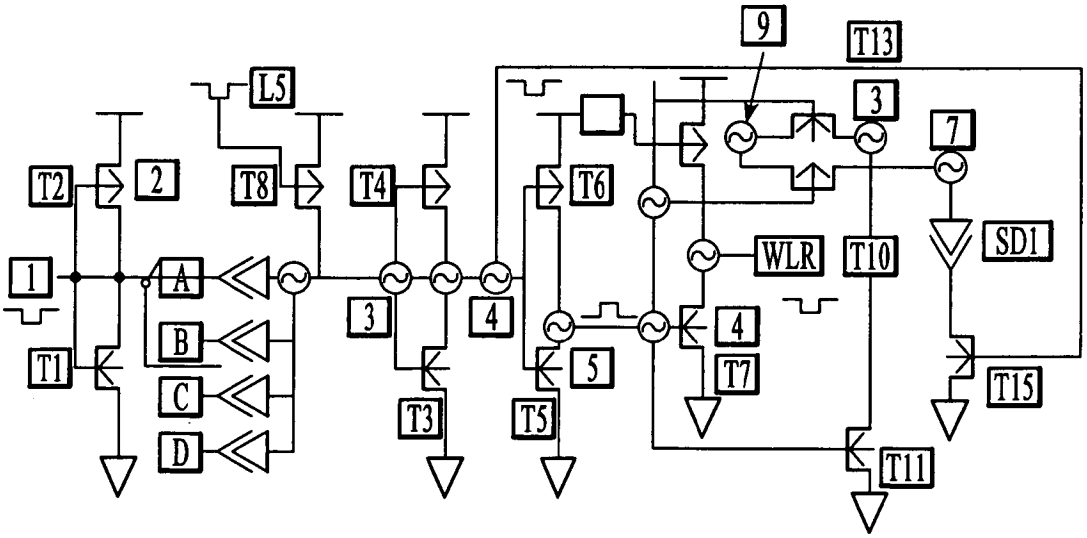


FIG.23D